1. General Description

This 8-bit Micro-controller uses a fully static CMOS technology to achieve high speed, small size, low power and high noise immunity.

On chip memory includes 4 K words of Flash ROM, and 256 bytes of EEPROM, and 256 bytes of static RAM.

2. Features

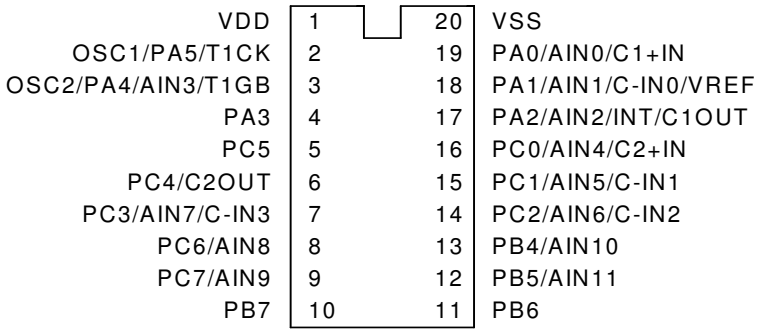
- Fully CMOS static design
- 8-bit data bus
- On chip flash ROM size :
  CYICT90F685 -- 4 K words
- Internal RAM size :
  CYICT90F685 -- 256 bytes
  (256 general purpose registers)
- 256 bytes of EEPROM
- 37 single word instructions
- 14-bit instructions
- 8-level stacks
- Operating voltage : 2.3V ~ 5.5 V
- Watchdog timer with on-chip RC oscillator
- Interrupt capability
- A/D converter module:
- 12 analog input multiplexed into one A/D converter with 8-bit resolution
- Timer0 : 8-bit timer with 3-bit prescaler
- Timer1 : 16-bit timer with 2-bit prescaler
- Timer2 : 8-bit timer
- Capture，Compare，PWM module
- two analog comparator module
- Sleep mode for power saving
- PA,PB with port change wake-up interrupt
- Power-on Reset
- 18 I/O pins with their own independent direction control

3. Applications

The application areas of this CYICT90F685 range from appliance motor control and high speed automotive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral … etc.

4. Pin Assignment

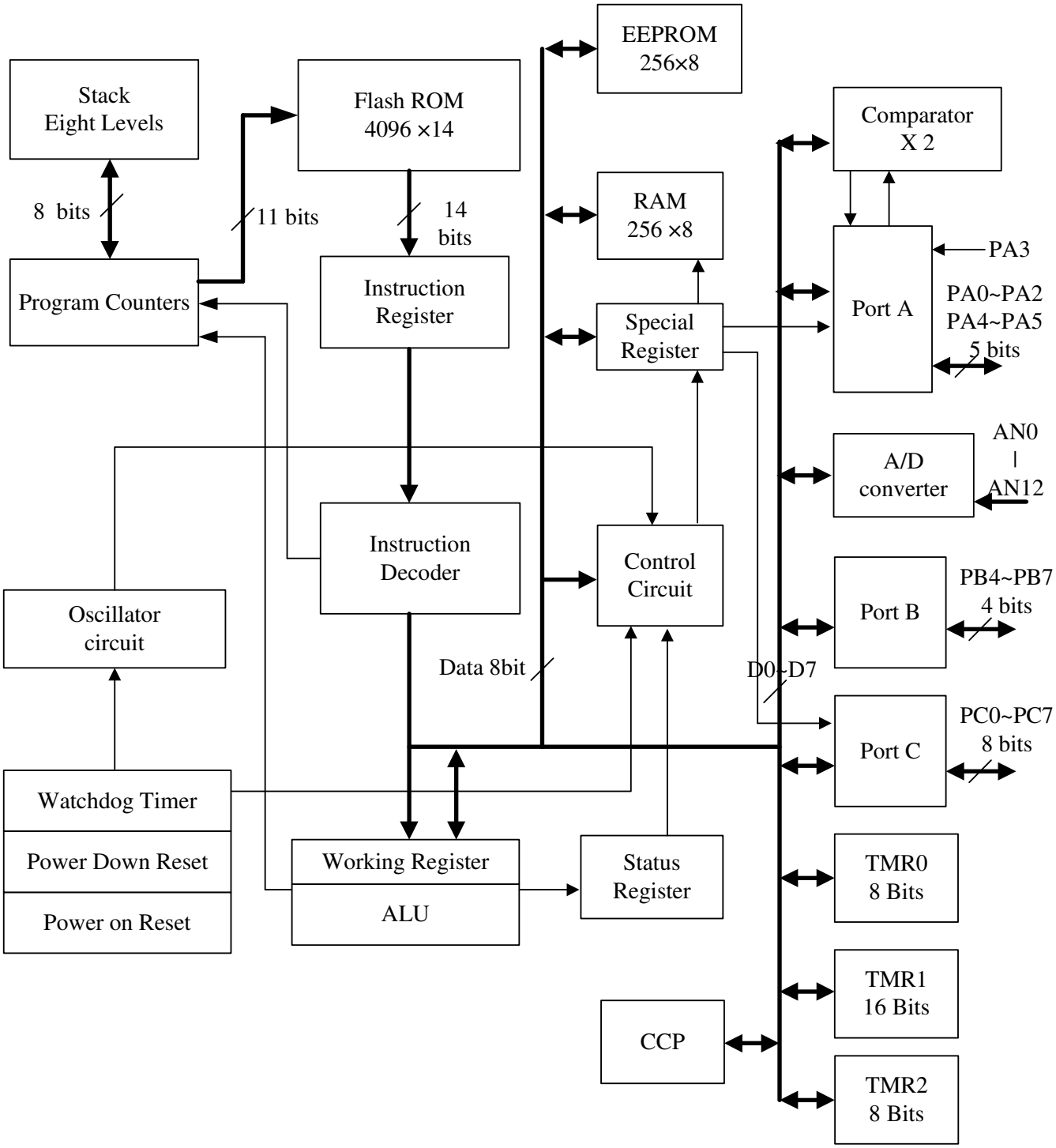
CYICT90F685P11/S11/SS11



5. Order Information

Device	ROM (Words)	RAM (Bytes)	EEPROM (Bytes)	I/O	A/D CH.	Comparators	Timer (8/16 bit)	Package	REMARK
CYICT90F685P11	4.0K	256	256	18	12	2	2/1	20-DIP	PIN4 IS PA3 FUNC.
CYICT90F685S11	4.0K	256	256	18	12	2	2/1	20-SOP	
CYICT90F685SS11	4.0K	256	256	18	12	2	2/1	20-SSOP	

6. Block Diagram

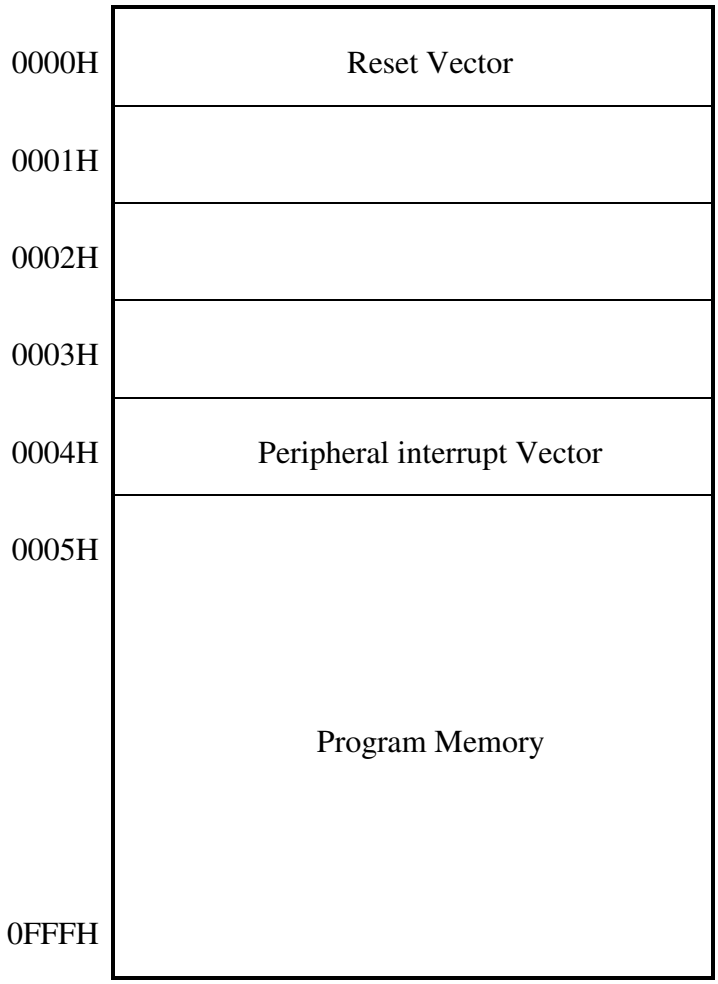


7. Pin Function Description

Pin name	Type	Buffer type	Description	
PA0/C1+IN/AIN0	I/O	TTL	TTL input level , with program pull_hi and interrupt on pin change.	Comparator1 + input. A/D Channel 0 input.
PA1/C-IN0/AIN1/Vref	I/O	TTL		Comparator – input0. A/D Channel 1 or Vref input.
PA2/T0CK/INT/ C1OUT/AIN2	I/O	TTL		Timer0 clock input. External interrupt. Comparator1 output. A/D Channel 2 input.
PA3/VPP	I	TTL/ST	TTL input level, with program interrupt on pin change.	VPP as Schmitt Trigger input level.
PA4/OSC2/T1GB/AIN3	I/O	TTL/ST	TTL input level , with program pull_hi and interrupt on pin change.	Oscillator crystal output, in RCmode clock output Fosc/4 frequency. Timer1 gate. Schmitt Trigger inputlevel A/D Channel 3 input.
PA5/OSC1/T1CKI	I/O	TTL/ST		Oscillator crystal input/external clock source input. Timer1 clock input. Schmitt Trigger input level.
PB4/AIN10	I/O	TTL	TTL input level, with program pull_hi and interrupt on pin change.	PB4 can be A/D Channel 10 input
PB5/AIN11	I/O	TTL		PB5 can be A/D Channel 11 input
PB6	I/O	TTL		Bi-directional I/O port
PB7	I/O	TTL		Bi-directional I/O port
PC0/C2+IN/AIN4	I/O	TTL	Port C, TTL input level.	Comparator2 + input A/D Channel 4 input.
PC1/C-IN1/AIN5	I/O	TTL		Comparator – input1. A/D Channel 5 input.
PC2/C-IN2/C1D/AIN6/	I/O	TTL		Comparator – input2. PWM D output A/D Channel 6 input
PC3/C-IN3/P1C/AIN7/ C1C	I/O	TTL		Comparator – input3. PWM C output A/D Channel 7 input.
PC4/C2OUT/C1B	I/O	TTL		Comparator2 output. PWM B output
PC5/CCP1/C1A	I/O	TTL		TTL input level. Caputre input/Compare output PWM A output
PC6/AIN8	I/O	TTL		A/D Channel 8 input.
PC7/AIN9	I/O	TTL		A/D Channel 9 input.
Vdd			Power supply	
Vss			Ground	

8. Memory Map

8.1 Program memory :



8.2 Register file map :

	BANK 0	BANK 1	
00h	IADD	IADD	80h
01h	TMR0	OPTR	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	RSR	RSR	84h
05h	Port A	PTIO A	85h
06h	Port B	PTIO B	86h
07h	Port C	PTIO C	87h
08h			88h
09h			89h
0Ah	PCH	PCH	8Ah
0Bh	INTCTL	INTCTL	8Bh
0Ch	PIF1	PIE1	8Ch
0Dh	PIF2	PIE2	8Dh
0Eh	TMR1L	PWCTL	8Eh
0Fh	TMR1H	OSCCTL	8Fh
10h	T1CTL	EOSCCTL	90h
11h	TMR2		91h
12h	T2CTL	PR2	92h
13h			93h
14h			94h
15h	CCP1L	PAPHR	95h
16h	CCP1H	PAINTR	96h
17h	CCP1CTL	WDTCTL	97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch	PWM1CTL		9Ch
1Dh	CCPAS		9Dh
1Eh	ADRESH	ADRESL	9Eh
1Fh	ADCTL0	ADCTL1	9Fh
20h	General Purpose Register	General Purpose Register	A0h
			EFh
		Access	F0h
7Fh		70h~7Fh	FFh

	BANK 2	BANK 3	
100h	IADD	IADD	180h
101h	TMR0	OPTR	181h
102h	PCL	PCL	182h
103h	STATUS	STATUS	183h
104h	RSR	RSR	184h
105h	Port A	PTIO A	185h
106h	Port B	PTIO B	186h
107h	Port C	PTIO C	187h
108h			188h
109h			189h
10Ah	PCH	PCH	18Ah
10Bh	INTCTL	INTCTL	18Bh
10Ch	EEDATA	EECTL1	18Ch
10Dh	EEADR	EECTL2	18Dh
10Eh			18Eh
10Fh			18Fh
110h			190h
111h			191h
112h			192h
113h			193h
114h			194h
115h	PBPHR		195h
116h	PBINTR		196h
117h			197h
118h	VRCTL		198h
119h	CM1CTL0		199h
11Ah	CM2CTL0		19Ah
11Bh	CM2CTL1		19Bh
11Ch			19Ch
11Dh		PSTRCTL	19Dh
11Eh	ADINSL	SRCTL	19Eh
11Fh	ADINSH		19Fh
120h	General Purpose Register		1A0h
			1EFh
17Fh	Access	Access	1F0h
17Fh	70h~7Fh	70h~7Fh	1FFh

Unimplemented memory location.

CYICT90F685 REGISTER FILE SUMMARY

Address	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BANK0									
00	**IADD**	Addressing this location uses the content of RSR to address data memory (not a physical register)							
01	**TMR0**	8 Bit Real time clock / counter							
02	**PCL**	Low order 8 bit of PC							
03	**STATUS**	RPS2	RPS1	RPS0	/TO	/PL	Z	HC	C
04	**RSR**	Indirect Register Address pointer							
05	**PORT A**	-	-	PA5	PA4	PA3	PA2	PA1	PA0
06	**PORT B**	PB7	PB6	PB5	PB4				
07	**PORT C**	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
0A	**PCHLAT**				Write buffer for high byte of PC				
0B	**INTS**	GIE	PEIE	T0IE	INTIE	PABIE	T0IF	INTIF	PABIF
0C	**PIF1**	-	ADIF	-	-	-	CCP1IF	TMR2IF	TMR1IF
0D	**PIF2**	-	C2IF	C1IF	EEIF				-
0E	**TMR1L**	Timer 1 Least Significant Byte							
0F	**TMR1H**	Timer 1 Most Significant Byte							
10	**T1CTL**	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	/T1SYNC	TMR1CLK	TMR1ON
11	**TMR2**				TMR2	REGISTER			
12	**T2CTL**	-	-	-	-	-	TMR2ON	T2CKPS1	T2CKPS0
15	**CCP1L**	CCP1 Least Significant Byte							
16	**CCP1H**	CCP1 Most Significant Byte							
17	**CCP1CTL**	P1M1	P1M0	PWM1L1	PWM1L0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
1C	**PWM1CTL**	PRESE	PWMD6	PWMD5	PWMD4	PWMD3	PWMD2	PWMD1	PWMD0
1D	**CCPAS**	CCPASE	CCPAS2	CCPAS1	CCPAS0	PSDAC1	PSDAC0	PSDBD1	PSDBD0
1E	**ADRESH**		A/D	Result	register	high	byte		
1F	**ADCTL0**	ADFS	ADRS	CHS3	CHS2	CHS1	CHS0	GO/DONEB	ADON
BANK1									
81	**OPTR**	PABPH	INTES	T0CS	T0SE	PSS	PS2	PS1	PS0
85	**PTIO A**	-	-		PORTA	DATA	DIRECTION	REGISTER	
86	**PTIO B**	PORTB	DATA	DIRECTION	REGISTER				
87	**PTIO C**			PORTC	DATA	DIRECTION	REGISTER		
8C	**PIE1**	-	ADIE	-	-	-	CCP1IE	TMR2IE	TMR1IE
8D	**PIE2**	-	C2IE	C1IE	EEIE	-	-	-	-
8E	**PWCTL**	-	-	-	-	-	-	PORB	-
8F	**OSCCTL**	LRCE	IRCS2	IRCS1	IRCS0	-	-	-	OSCIN
90	**EOSCCTL**	ENINF	-	-	-	ECKIN	OSO2E	OSC2O	-
92	**PR2**			TMR2	Period	Register			
95	**PAPHR**	-	-	PAH5	PAH4	-	PAH2	PAH1	PAH0
96	**PAINTR**	-	-	PINTA5	PINTA4	PINTA3	PINTA2	PINTA1	PINTA0
97	**WDTCTL**	-	-	-	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTE
9E	**ADRESL**		A/D	Result	register	low	byte		
9F	**ADCTL1**	-	ASCS2	ASCS1	ASCS0	-	-	-	-
BANK2									
10C	**EEDATA**			EEPROM	DATA	REGISTER			
10D	**EEADR**			EEPROM	ADDRESS	REGISTER			
115	**PBPHR**	PBH7	PBH6	PBH5	PBH4	-	-	-	-
116	**PBINTR**	PINTB7	PINTB6	PINTB5	PINTB4	-	-	-	-
118	**VRCTL**	C1VRE	C2VRE	CVRRS	FVRE	CVR3	CVR2	CVR1	CVR0
119	**CM1CTL0**	CM1ON	CM1OUT	CM1OE	C1INV	-	CM1R	CM1S1	CM1S0
11A	**CM2CTL0**	CM2ON	CM2OUT	CM2OE	C2INV	-	CM2R	CM2S1	CM2S0
11B	**CM2CTL1**	CM1OUT	CM2OUT	-	-	-	-	T1GSS	C2SYNC
11E	**ADINSL**	AINS7	AINS6	AINS5	AINS4	AINS3	AINS2	AINS1	AINS0
11F	**ADINSH**	-	-	-	-	AINS11	AINS10	AINS9	AINS8

BANK3									
18C	**EECTL1**	-	-	-	-	WRERR	WREN	WR	RD
18D	**EECTL2**			EEPROM	control	Register	2		
19D	**PSTRCTL**	-	-	-	STRSYNC	STRED	STREC	STREB	STREA
19E	**SRCTL**	SR1	SR0	CM1SEN	CM2SEN	PULSS	PULSR	-	-

00H、80H、100H、180H : IAR (Indirect Address Register)

Use contents of RSR to address data memory (not a physical register)

(1).01H、101H : TMR0 (Timer0 Counter).

8-bit real time clock/counter

(2).02H、82H、102H、182H : PCL (Program Counter Low Byte)

Low order 8 bits of the Program Counter (PC)

(3).03H、83H、103H、183H: STATUS (Status register).

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
STATUS	PRS2	RPS1	RPS0	/TO	/PL	Z	HC	C

Bit	**Symbol**	**Function**
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	/PL	Power loss Flag bit
4	/TO	WDT TIME OUT bit
5	RPS0	Register page select bit 0 0： 00/H --- 7F/H 0 1： 80/H --- FF/H 1 0：100/H --- 17F/H 1 1：180/H --- 1FF/H
6	RPS1	
7	RPS2	Register page select bit 0： 00/H--- FF/H 1：100/H---1FF/H

(4).04H、84H、104H、184H : RSR (Memory Select Register)

Indirect data memory address pointer.

(5).05H、105H : Port A data output register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port A	-	-	PA5	PA4	PA3	PA2	PA1	PA0

Bit 7 – 6 : Unimplemented
Bit 5 – 0 : PA5 ~ PA0 , I/O Register

(6).06H、106H : Port B data output register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port B	PB7	PB6	PB5	PB4	-	-	-	-

(7).07H、107H : Port C data output register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port C	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(8).08 ~ 09H : Unimplemented Register.

(9).0AH、8AH、10AH、18AH : Program counter high byte.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCHLAT	-	-	-	PCH4	PCH3	PCH2	PCH1	PCH0

(10). 0BH、8BH、10BH、18BH : Interrupt control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTS	GIE	PEIE	T0IE	INTIE	PABIE	T0IF	INTIF	PABIF

Bit	Symbol	Function
0	PABIF	PA,PB Port Change Interrupt Flag Bit. 0 = None of the PA,PB pins have changed state 1 = When at least one of the PA,PB pins changed state (must be cleared in software)
1	INTF	PA2/INT Interrupt Flag Bit. 0 = The PA2/INT interrupt did not occur 1 = The PA2/INT interrupt occurred
2	T0IF	TMR0 Overflow Interrupt Flag Bit. 0 = Timer0 did not overflowed 1 = Timer0 has overflowed (must be cleared in software)

Bit	Symbol	Function
3	PABIE	PA,PB Port Change Interrupt Enable Bit. 0 ： disable PA,PB change interrupt 1 ： enable PA,PB change interrupt
4	INTIE	INT Pin Interrupt Enable Bit. 0 ： disable INT interrupt 1 ： enable INT interrupt
5	T0IE	TMR0 Overflow Interrupt Enable Bit. 0 ： disable TMR0 interrupt 1 ： enable TMR0 interrupt
6	PEIE	Peripheral Interrupt Enable Bit. 0 ： disable all peripheral interrupt 1 ： enable all peripheral interrupt
7	GIE	Global Interrupt Enable Bit. 0 ： disable global interrupt 1 ： enable global interrupt

(11). 0CH : PIF1 (Peripheral interrupt register1).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIF1	-	ADIF	-	-	-	CCP1IF	TMR2IF	TMR1IF

Bit	Symbol	Function
0	TMR1IF	TMR1 Overflow Interrupt Flag Bit. 0 = Timer1 register did not overflow 1 = Timer1 register overflowed (must be cleared in software)
1	TMR2IF	TMR2 Overflow Interrupt Flag Bit. 0 = Timer2 register did not overflow 1 = Timer2 register overflowed (must be cleared in software)
2	CCP1IF	CCP1 interrupt flag 0: No TMR1 capture/compare occurred 1: A TMR1 capture/compare occurred
3~5	-	-
6	ADIF	A/D interrupt flag bit. 0 = A/D conveter not complete 1 = A/D conveter complete
7	-	

(12). 0DH : PIF2 (Peripheral interrupt register2).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIF2	-	CMP2IF	CMP1IF	EEIF	-	-	-	-

Bit	Symbol	Function
0~3	-	-
4	EEIF	EE interrupt flag bit. 0 = EE operation has not completed 1 = EE operation has completed
5	CMP1IF	Comparator1 interrupt flag bit. 0 = CMP1 output has not changed 1 = CMP1 output has changed
6	CMP2IF	Comparator2 interrupt flag bit. 0 = CMP2 output has not changed 1 = CMP2 output has changed
7	-	

(13). 0EH : TMR1L (The timer1 LSB register)

The LSB of the 16-bit TMR1.

(14). 0FH : TMR1H (The timer1 MSB register)

The MSB of the 16-bit TMR1.

10H : Timer1 control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1CTL	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	/T1SYNC	TMR1CLK	TMR1ON

Bit	Symbol	Function
0	TMR1ON	0 = Stop TMR1 1 = Enable TMR1
1	TMR1CLK	0 = Internal clock (Fosc/4) 1 = External clock from pin PC0
2	$\overline{\text{T1SYNC}}$	TMR1CLK = 1 0 = Synchronize external clock 1 = Do not synchronize external clock TMR1CLK = 0 This bit is ignored
3	T1OSCEN	If INTOSC without CLKOUT oscillator is active : 0 = LP oscillator is off 1 = LP oscillator is enabled for Timer1 clock
4~5	T1CKPS1 ~ T1CKPS0	0 0 = 1：1 Prescale value 0 1 = 1：2 Prescale value 1 0 = 1：4 Prescale value 1 1 = 1：8 Prescale value

Bit	Symbol	Function
6	TMR1GE	TMR1 gate control enable bit TMR1ON=0，this bit is ignored TMR1ON=1 0 = gate control disable 1 = gate control enable
7	T1GINV	TMR1 gate invert bit 0 = active low 1 = active high

(15). 11 H：TMR2

TMR2 register

(16). 12H：T2CTL(Timer2 control register.)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CTL	-	-	-	-	-	TMR2ON	T2CKPS1	T2CKPS0

Bit	Symbol	Function
0-1	T2CKPS 1~0	0 0 = 1：1 Prescale value 0 1 = 1：2 Prescale value 1 0 = 1：4 Prescale value 1 1 = 1：8 Prescale value
2	TMR2ON	0 = Stop TMR2 1 = Enable TMR2
3~7	-	-

(17). 13 ~ 14H : Unimplemented register.

(18). 15H：**CCP1L**

Capture/Compare/PWM LSB

(19). 16H：**CCP1H**

Capture/Compare/PWM MSB

(20). 17H：**CCP1CTL**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CCP1CTL	P1M1	P1M0	PWM1L1	PWM1L0	CCP1M3	CCP1M2	CCP1M1	CCP1M0

Bit	Symbol	Function
3~0	CCP1M3 ~ CCP1M0	CCP1 Mode select 0 0 0 0 : CCP1 off 0 0 1 0 : Compare mode,toggle output on match 0 1 0 0 : Capture1 mode, every falling edge 0 1 0 1 : Capture1 mode, every rising edge 0 1 1 0 : Capture1 mode, every 4th rising edge 0 1 1 1 : Capture1 mode, every 16th rising edge 1 0 0 0 : Compare1 mode, set output on match 1 0 0 1 : Compare1 mode, clear output on match 1 0 1 0 : Compare1 mode, generate software interrupt on match 1 0 1 1 : Compare1 mode, trigger special event 1 1 0 0 : PWM mode , P1A,C active-High ; P1B,D active-High 1 1 0 1 : PWM mode , P1A,C active-High ; P1B,D active-Low 1 1 1 0 : PWM mode , P1A,C active-Low ; P1B,D active-High 1 1 1 1 : PWM mode , P1A,C active-Low ; P1B,D active-Low
5~4	PWM1L1 ~ PWM1L0	These bits are the two LSBs of the PWM1 duty cycle
7~6	P1M1 ~ P1M0	PWM1 Mode select when 1、CCP1M<3:2> = 00 , 01 , 10 P1A = Capture/Compare input。P1B,C,D as port. 2、CCP1M<3:2> = 11, 0 0 : Single output. 0 1 : Full-bridge forward output. 1 0 : Half-bridge output. 1 1 : Full-bridge reverse output.

(21). 18 ~ 1BH : Unimplemented register.

(22). 1CH：**PWM1CTL** (PWM1 control register.)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1CTL	PRESE	PWMD6	PWMD5	PWMD4	PWMD3	PWMD2	PWMD1	PWMD0

Bit	Symbol	Function
6~0	PWMD6 ~ PWMD0	PWM Delay bit . Delay time = (Fosc/4) x PWMD<6:0>
7	PRESE	PWM Reset enable bit . 0 : CCPASE must be cleared in software 1 : CCPASE automatically clear when shutdown event goes away.

(23). 1DH：CCPAS (CCP auto shutdown control register.)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CCPAS	CCPASE	CCPAS2	CCPAS1	CCPAS0	PSDAC1	PSDAC0	PSDBD1	PSDBD0

Bit	Symbol	Function
1~0	PSDBD1 ~ PSDBD0	P1B,P1D Shutdown state control bit . 0 0 : P1B,P1D Drive to 0 0 1 : P1B,P1D Drive to 1 1 x : P1B,P1D as tri-state
3~2	PSDAC1 ~ PSDAC0	P1A,P1C Shutdown state control bit . 0 0 : P1A,P1C Drive to 0 0 1 : P1A,P1C Drive to 1 1 x : P1A,P1C as tri-state
6~4	CCPAS2 ~ CCPAS0	CCP auto-shutdown source select bit 0 0 0 : disable 0 0 1 : CMP1 output change 0 1 0 : CMP2 output change 0 1 1 : CMP1 or CMP2 output change 1 0 0 : INT on Low 1 0 1 : INT on Low or CMP1 output change 1 1 0 : INT on Low or CMP2 output change 1 1 1 : INT on Low or CMP1 or CMP2 output change
7	CCPASE	CCP auto-shutdown status bit 0 : CCP are operating 1 : CCP shutdown has occurred.

(24). 1EH : ADRESH (Most A/D result register.)

A/D result most 8 bits or 2 bits

(25). 1FH : ADCTL0 (A/D control register 0).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCTL0	ADFS	ADRS	CHS3	CHS2	CHS1	CHS0	G0/DONE	ADRUN

Bit	Symbol	Function
0~1	ADRUN	A/D conversion enable bit. 0 = A/D converter is shut-off. 1 = A/D converter operating.
1	G0/DONE	A/D conversion status bit. 0 = A/D conversion completed/not in progress 1 = A/D conversion cycle in progress. Setting this bit start A/D conversion cycle. This bit is automatically cleared by hardware when A/D has completed.
2~5	CHS3 ~ CHS0	Analog channel select bits. 0 0 0 0 = Channel AN0 (PA0) 0 0 0 1 = Channel AN1 (PA1) 0 0 1 0 = Channel AN2 (PA2) 0 0 1 1 = Channel AN3 (PA4) 0 1 0 0 = Channel AN4 (PC0) 0 1 0 1 = Channel AN5 (PC1) 0 1 1 0 = Channel AN6 (PC2) 0 1 1 1 = Channel AN7 (PC3) 1 0 0 0 = Channel AN8 (PC6) 1 0 0 1 = Channel AN9 (PC7) 1 0 1 0 = Channel AN10 (PB4) 1 0 1 1 = Channel AN11 (PB5) 1 1 0 0 = CVref 1 1 0 1 = 0.6v Vref
6	ADRS	A/D voltage referece bit. 0 = Vdd 1 = Vref pin
7	ADFS	A/D result formed select bit. 0 = Left justified 1 = Right justified

*Suggest ADFS = 0 to use 8-bit resolution

(26). 81H : OPTR (Option control register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTR	/PABPH	INTES	T0CS	T0SE	PSS	PS2	PS1	PS0

Bit	Symbol	Function		
2~0	PS2 ~ PS0	Prescaler Value	TMR0 rate	WDT rate
		0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSS	Prescaler assignment bit : 0 = Timer 0 1 = Watchdog Timer		
4	T0SE	TMR0 signal Edge : 0 = Increment on low-to-high transition on PA2 pin 1 = Increment on high-to-low transition on PA2 pin		
5	T0CS	TMR0 signal set : 0 = Internal instruction cycle clock 1 = Transition on PA2/INT pin		
6	INTES	PA2 interrupt edge select bit : 0 = Interrupt on falling edge of PA2/INT pin 1 = Interrupt on rising edge of PA2/INT pin		
7	/PABPH	Port A,B Pull-up Enable Bit : 0 = PA0~2 & PA4~5 & PB4~7 pull-up all enable 1 = PA0~2 & PA4~5 & PB4~7 pull-up all disable		

(27). 85H : Port A input/output control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PTIO A	-	-	PTIO PA5	PTIO PA4	PTIO PA3	PTIO PA2	PTIO PA1	PTIO PA0

(28). 86H : Port B input/output control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PTIO B	PTIO PB7	PTIO PB6	PTIO PB5	PTIO PB4	-	-	-	-

(29). 87H : Port C input/output control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PTIO C	PTIO PC7	PTIO PC6	PTIO PC5	PTIO PC4	PTIO PC3	PTIO PC2	PTIO PC1	PTIO PC0

(30). 88H ~ 89H : Unimplemented register.

(31). 8CH : PIE1 (Peripheral interrupt enable register1).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIE1	-	ADIE	-	-	-	CCP1IE	TMR2IE	TMR1IE

Bit	Symbol	Function
0	TMR1IE	TMR1 Overflow Interrupt Enable Bit. 0 = Disable the TMR1 overflow interrupt 1 = Enable the TMR1 overflow interrupt
1	TMR2IE	TMR2 Overflow Interrupt Enable Bit. 0 = Disable the TMR2 overflow interrupt 1 = Enable the TMR2 overflow interrupt
2	CCPIE	CCP1 Interrupt Enable Bit. 0 = Disable CCP1 interrupt 1 = Enable CCP1 interrupt
5~3	-	-
6	ADIE	A/D interrupt enable bit. 0 = disable A/D interrupt 1 = enable A/D interrupt
7	-	-

(32). 8DH : PIE2 (Peripheral interrupt enable register2).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIE2	-	CM2IE	CM1IE	EEIE	-	-	-	-

Bit	Symbol	Function
3~0	-	-
4	EEIE	EEPROM Write Operation Interrupt Enable Bit. 0 = Disable the EEPROM write complete interrupt 1 = Enable the EEPROM write complete interrupt
5	CM1IE	Comparator1 Interrupt Enable Bit. 0 = Disable the comparator interrupt 1 = Enable the comparator interrupt
6	CM2IE	Comparator2 Interrupt Enable Bit. 0 = Disable the comparator interrupt 1 = Enable the comparator interrupt
7	-	-

(33). 8EH : PWCTL (Power control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWCTL	-	-	-	-	-	-	PORB	-

PORB : Power On Reset Status Bit.
0 = A power on reset occurred
(must be set in software after a power on reset occurs)
1 = No power on reset occurred

(34). 8FH : OSCCTL (oscillator control segister)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSCCTL	LRCE	IRCS2	IRCS1	IRCS0	-	-	-	OSCIN

Bit	Symbol	Function
0	OSCIN	MCU Internal Or external oscillator Select Bit. 0 = MCU clock based on external oscillator (type from option select) 1 = MCU clock based on internal oscillator **When internal oscillator change to external oscillator must wait OST time 20ms.**
3~1	-	-
6~4	IRCS2 ~ IRCS0	Internal RC select Bit. 0 0 0 = 32 kHz 0 0 1 = 128 kHz 0 1 0 = 256 kHz 0 1 1 = 512 kHz 1 0 0 = 1 MHz 1 0 1 = 2 MHz 1 1 0 = 4 MHz(default) 1 1 1 = 8 MHz
7	LRCE	Slow IRC 128k enable bit when IRCS2~0 = 0 0 1 0 = internal RC select high power RC 1 = internal RC select low power RC **and close HIRC**

(35). 90H : EOSCCTL (external oscillator control register.)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EOSCCTL	ENINF	-	-	-	ECKIN	OSO2E	OSC2O	-

Bit	Symbol	Function
0	-	-
1	OSC2O	OSC2 Oscillator Clock Output Enable Bit. 0 = Disable OSC2 oscillator clock output in internal or external of RC mode oscillator 1 = Enable OSC2 oscillator clock output in internal or external of RC mode oscillator
2	OSO2E	Both of highspeed-Internal and external oscillator Enable Bit. 0 = Only use internal oscillator or external oscillator 1 = Internal and external (LF mode only) oscillator enable both
3	ECKIN	External Clock Input Enable Bit. 0 = Disable oscillator external clock input 1 = Enable oscillator external clock input (must be set in external oscillator of RC mode)
6~4	-	-
7	ENINF	Enable internal RC flag Bit.

(36). 91H ~ 94H : Unimplemented register.

(37). 95H : PAPHR (Port A pull_hi control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAPHR	-	-	PHA5	PHA4	-	PHA2	PHA1	PHA0

Bit 5-4 & Bit 2-0 : Port A Pull_hi Control Bits
0 = Pull_hi disable
1 = Pull_hi enable

(38). 96H : PAINTR (Port A interrupt-on-change control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAINTR	-	-	PINTA5	PINTA4	PINTA3	PINTA2	PINTA1	PINTA0

Bit 5-0 : Port A Interrupt-On-Change Control Bits
0 = Interrupt-on-change disable
1 = Interrupt-on-change enable

(39). 97H WDTCTL (WDT control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTCTL	**-**	**-**	-	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTE

Bit	Symbol	Function
0	SWDTE	Software WDT enable bit when WDTE = 0 0 = wdt is off 1 = wdt is enable ***If WDTE = 1 ,WDT always = 1**
4~1	WDTPS2 ~ WDTPS0	WDT period select bit.

WDTPS2~PS0	period	WDTPS2~PS0	period
0 0 0 0	1:32	0 1 1 1	1:4096
0 0 0 1	1:64	1 0 0 0	1:8192
0 0 1 0	1:128	1 0 0 1	1:16384
0 0 1 1	1:256	1 0 1 0	1:32768
0 1 0 0	1:512	1 0 1 1	1:65536
0 1 0 1	1:1024	1 1 X X	reserved
0 1 1 0	1:2048		

7~5	-	-

(40). 98H ~ 9DH : Unimplemented register.

(41). 9EH : ADRESL (Least A/D result register).

A/D result least 8 bits or 2 bits

(42). 9FH : ADCTL1 (A/D control register 1).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCTL1	**-**	ASCS2	ASCS1	ASCS0	**-**	**-**	**-**	**-**

Bit	Symbol	Function
3~0	-	**-**
6~4	ASCS2 ~ ASCS0	A/D conversion clock select bits. 0 0 0 = Fosc/2 0 0 1 = Fosc/8 0 1 0 = Fosc/32 X 1 1 = Select by external oscillator mode. RC & LF = Fosc/2; XT = Fosc/8; HF = Fosc/32 1 0 0 = Fosc/4 1 0 1 = Fosc/16 1 1 0 = Fosc/64
7	-	-

ASCS2,0	TAD	Oscillator frequency	Minimum TAD	Oscillator frequency	Maximum TAD	Type	Remark
000	Fosc / 2	1M Hz	2us	200K Hz	10us	LF,RC	
001	Fosc / 8	4M Hz	2us	1M Hz	8us	XT	
010	Fosc /32	20M Hz	1.6us	4M Hz	8us	HF	
100	Fosc / 4	2M Hz	2us	250K Hz	8us	LF,RC	
101	Fosc /16	8M Hz	2us	2M Hz	8us	XT	
110	Fosc /64	20M Hz	3.2us	8M Hz	8us	HF	
X11	RC:Fosc / 2	1M Hz	2us	200K Hz	10us	RC	
	LF:Fosc / 2	1M Hz	2us	200K Hz	10us	LF	
	XT:Fosc / 8	4M Hz	2us	1M Hz	8us	XT	
	HF:Fosc/32	20M Hz	1.6us	4M Hz	8us	HF	

The A/D conversion clock (1/TAD) must be select to ensure a TAD between minimum 1.6us and maximum 8us

(43). 10CH : EEDATA (EEPROM data register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEDATA	EED7	EED6	EED5	EED4	EED3	EED2	EED1	EED0

(44). 10DH : EEADR (EEPROM address register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEADR	EEAD7	EEAD6	EEAD5	EEAD4	EEAD3	EEAD2	EEAD1	EEAD0

(45). 115H : PBPHR (Port B pull_hi control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBPHR	PHB7	PHB6	PHB5	PHB4	-	-	-	-

Bit 7-4 : Port B Pull_hi Control Bits
0 = Pull_hi disable
1 = Pull_hi enable

(46). 116H : PBINTR (Port B interrupt-on-change control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAINTR	PINTB7	PINTB7	PINTB5	PINTB4	-	-	-	-

Bit 7-4 : Port B Interrupt-On-Change Control Bits
0 = Interrupt-on-change disable
1 = Interrupt-on-change enable

(47). 118H : VRCTL (Voltage reference control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VRCTL	C1VRE	C2VRE	CVRRS	FVRE	CVR3	CVR2	CVR1	CVR0

Bit	Symbol	Function
3~0	CVR3 ~ CVR0	Comparator Voltage Reference Value Selection When CVRRS = 0, CVref = Vdd/4 + (CVR3:CVR0/32)*Vdd When CVRRS = 1, CVref = (CVR3:CVR0/24)*Vdd
4	FVRE	Fixed reference enable bit 0 = disable 1 = enable
5	CVRRS	Comparator Voltage Reference Range Select Bit 0 = High range ; CVref = Vdd/4 + (CVR3:CVR0/32)*Vdd 1 = Low range ; CVref = (CVR3:CVR0/24)*Vdd
6	C2VRE	Comparator2 Voltage Reference Enable Bit 0 = fixedverf connect to C2vref input 1 = Cvref on and connect to C2vref input
7	C1VRE	Comparator1 Voltage Reference Enable Bit 0 = fixedverf connect to C1vref input 1 = Cvref on and connect to C1vref input

(48). 119H : CM1CTL0 (Comparator 1 control register0).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CM1CTL0	CM1ON	CM1OUT	CM1OE	C1INV	-	CM1R	CM1CH1	CM1CH0

Bit	Symbol	Function
1~0	CM1CH0 ~ CM1CH1	Comparator 1 channel select 0 0 = CM1Vin- connects to C-IN0 PIN 0 1 = CM1Vin- connects to C-IN1 PIN 1 0 = CM1Vin- connects to C-IN2 PIN 1 1 = CM1Vin- connects to C-IN3 PIN
2	CM1R	Comparator 1 Referenct select 0 = C1+ connected to C1+IN pin 1 = C1+ connected to C1VREF
3	-	-
4	C1INV	Comparator 1 output Inversion Bit 0 = Output not inverted 1 = Output inverted
5	CM1OE	Comparator 1 Output Enable bit 1 = PA2 as C1OUT pin 0 = C1OUT is internal only

Bit	Symbol	Function
6	CM1OUT	Comparator Output Bit. When C1INV = 0 1 = Vin+ > Vin- ; 0 = Vin+ < Vin- When C1INV = 1 1 = Vin+< Vin- ; 0 = Vin+ > Vin-
7	CM1ON	Comparator 1 Enable bit 1 = Comparator 1 is enabled 0 = Comparator 1 is disabled

(49). 11AH : CM2CTL0 (Comparator 2 control register0).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CM2CTL0	CM2ON	CM2OUT	CM2OE	C2INV	-	CM2R	CM2CH1	CM2CH0

Bit	Symbol	Function
1~0	CM2CH0 ~ CM2CH1	Comparator 2 channel select 0 0 = CM2Vin- connects to C-IN0 PIN 0 1 = CM2Vin- connects to C-IN1 PIN 1 0 = CM2Vin- connects to C-IN2 PIN 1 1 = CM2Vin- connects to C-IN3 PIN
2	CM2R	Comparator 2 Referenct select 0 = C2+ connected to C2+IN pin 1 = C2+ connected to C2VREF
3	-	-
4	C2INV	Comparator 2 output Inversion Bit 0 = Output not inverted 1 = Output inverted
5	CM2OE	Comparator 2 Output Enable bit 0 = C2OUT is internal only 1 = PC4 as C2OUT pin
6	CM2OUT	Comparator 2 Output Bit. When C2INV = 0 1 = Vin+ > Vin- ; 0 = Vin+ < Vin- When C2INV = 1 1 = Vin+< Vin- ; 0 = Vin+ > Vin-
7	CM2ON	Comparator 2 Enable bit 0 = Comparator 2 is disabled 1 = Comparator 2 is enabled

(50). 11BH : CM2CTL1 (Comparator 2 control register1).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CM2CTL1	CM1OUT	CM2OUT	-	-	-	-	T1GSS	C2SYNC

Bit	Symbol	Function
0	C2SYNC	Comparator 2 Output Sync bit 0 = Output is asynchronous. 1 = Output is sync. to Timer1 falling edge.
1	T1GSS	Timer1 Gate Select bit. 0 = Timer1 gate is comparator 2 sync out. 1 = Timer1 gate is T1G pin
5~2	-	-
6	CM2OUT	Comparator 2 Output Bit.
7	CM1OUT	Comparator 1 Output Bit.

(51). 11EH : ADINSL (Analog input low channel select).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADINSL	AINS7	AINS6	AINS5	AINS4	AINS3	AINS2	AINS1	AINS0

0 = Digital I/O

1 = Analog input

(52). 11FH : ADINSH (Analog input high channel select).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADINSH	-	-	-	-	AINS11	AINS10	AINS9	AINS8

0 = Digital I/O

1 = Analog input

(53). 18CH : EECTL1 (EE control 1).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EECTL1	-	-	-	-	WRERR	WREN	WR	RD

Bit	Symbol	Function
0	RD	Read Control Bit. 0 = Does not initiate an EEPROM read. 1 = Initiates an EEPROM read (read takes once cycle. RD is cleared in hardwave. The RD bit can only be set (not clear) in software.)
1	WR	Write Control Bit. 0 = Write cycle to the data EEPROM is complete 1 = Initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not clear) in software.)
2	WREN	EEPROM Write Enable Bit. 0 = Inhibits write to the data EEPROM 1 = Allows write cycles
3	WRERR	EEPROM Write Error Flag Bit. 0 = The EEPROM write operation completed 1 = The EEPROM write operation is prematurely terminated (any MCLR reset or any WDT reset during normal operation)
7~4	-	-

(54). 18DH : EECTL2 (EE control 2).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EECTL2	-	-	-	-	-	-	-	-

Write only ; Read as “0”

When write data to the EEPROM must write 55/H to EECTL2,
and writ AA/H to EECTL2 then set WR bit;
the EEPROM can write data inside for write each byte.

Example : Data EEPROM Write

```
BSM     STATUS, RPS0 ;
BSM     STATUS, RPS1    ; Select bank 3
BCM     INTS, GIE       ; Disable interrupt
BSM     EECTL1, WREN    ; Enable write
MOVKW   55H
MOVWM   EECTL2          ; Write 55/H
MOVKW   0AAH
MOVWM   EECTL2          ; Write AA/H
BSM     EECTL1,WR       ; Begin write
```

(55). 19DH : PSTRCTL (PWM steering control register).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSTRCTL	-	-	-	STRSYNC	STRED	STREC	STREB	STREA

Bit	Symbol	Function
0	STREA	P1A Steering Enable bit 0 = P1A as I/O 1 = P1A as PWM output
1	STREB	P1B Steering Enable bit 0 = P1B as I/O 1 = P1B as PWM output
2	STREC	P1C Steering Enable bit 0 = P1C as I/O 1 = P1C as PWM output
3	STRED	P1D Steering Enable bit 0 = P1D as I/O 1 = P1D as PWM output
4	STRSYNC	Steering SYNC enable bit 0 = Steering output Not SYNC 1 = Steering output SYNC
7~5	-	-

(56). 19EH : SRCTL (SR latch control).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRCTL	SR1	SR0	CM1SEN	CM2SEN	PULSS	PULSR	-	-

Bit	Symbol	Function
0~1	-	-
2	PULSR	Reset SR latch bit. 0 = Not effect on SR latch 1 = Triggers pulse generator to reset SR latch,then immediately reset by hardware.
3	PULSS	Set SR latch bit. 0 = Not effect on SR latch 1 = Triggers pulse generator to set SR latch,then immediately reset by hardware.
4	CM2REN	Comparator 2 out reset enable bit 0 = Not effect on SR latch 1 = comparator 2 output sets SR latch
5	CM1SEN	Comparator 1 out set enable bit 0 = Not effect on SR latch 1 = comparator 1 output resets SR latch
6	SR0	Comparator 1 out select bit 0 = C1OUT pin is the comparator 1 output 1 = C1OUT pin is the latch Q

Bit	Symbol	Function
7	SR1	Comparator 2 out select bit 0 = C2OUT pin is the comparator 2 output 1 = C2OUT pin is the latch QN

9. Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IADD	00h(80h)	0000 0000	0000 0000	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h(82h)	0000 0000	0000 0000	0000 0100
STATUS	03h(83h)	0001 1xxx	000# #uuu	000# #uuu
RSR	04h(84h)	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	--xx xxxx	--uu uuuu	--uu uuuu
PORT B	06h	xxxx ----	xxxx ----	uuuu ----
PORT C	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCHLAT	0Ah(8Ah)	---0 0000	---0 0000	---u uuuu
INTS	0Bh(8Bh)	0000 0000	0000 0000	uuuu uuuu
PIF1	0Ch	-0-- -000	-0-- -000	-u-- -uuu
PIF2	0Dh	-000 ----	-000 ----	-uuu ----
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CTL	10h	-000 0000	-000 0000	-uuu uuuu
TMR2	11h	xxxx xxxx	uuuu uuuu	uuuu uuuu
T2CTL	12h	---- -000	---- -uuu	---- -uuu
CCP1L	15h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1H	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CTL	17h	0000 0000	0000 0000	uuuu uuuu
PWM1CTL	1Ch	0000 0000	0000 0000	uuuu uuuu
CCPAS	1Dh	0000 0000	0000 0000	uuuu uuuu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCTL0	1Fh	0000 0000	0000 0000	uuuu uuuu
OPTR	81h	1111 1111	1111 1111	uuuu uuuu
PTIO A	85h	--11 1111	--11 1111	--uu uuuu
PTIO B	86h	1111 ----	1111 ----	uuuu ----
PTIO C	87h	1111 1111	1111 1111	uuuu uuuu
PIE1	8Ch	-0-- -000	-0-- -000	-u-- -uuu
PIE2	8Dh	-000 ----	-000 ----	-uuu ----
PWCTL	8Eh	---- --#-	---- --u-	---- --u-
OSCCTL	8Fh	0110 ---1	0110 ---1	uuuu ---u
EOSCCTL	90h	x--- 000-	x--- 000-	u--- uuu-
PR2	92H	1111 1111	1111 1111	uuuu uuuu
PAPHR	95h	--11 -111	--11 -111	--uu -uuu
PAINTR	96h	--00 0000	--00 0000	--uu uuuu
WDTCTL	97h	---0 1000	---0 1000	---u uuuu

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
ADRESL	9Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCTL1	9Fh	-000 ----	-000 ----	-uuu ----
EEDATA	10Dh	0000 0000	0000 0000	uuuu uuuu
EEADR	10Eh	0000 0000	0000 0000	uuuu uuuu
PBPHR	115h	1111 ----	1111 ----	uuuu ----
PBINTR	116h	0000 ----	0000 ----	uuuu ----
VRCTL	118h	0000 0000	0000 0000	u-u- uuuu
CM1CTL0	119h	0000 -000	0000 -000	uuuu -uuu
CM2CTL0	11Ah	0000 -000	0000 -000	uuuu -uuu
CM2CTL1	11Bh	00-- --10	00-- --10	uu-- --uu
ADINSL	11Eh	1111 1111	1111 1111	uuuu uuuu
ADINSH	11Fh	---- 1111	---- 1111	uuuu uuuu
EECTL1	18Ch	---- #000	---- #000	---- #uuu
EECTL2	18Dh	---- ----	---- ----	---- ----
PSTRCTL	19Dh	---0 0001	---0 0001	---u uuuu
SRCTL	19Eh	0000 00--	0000 00--	uuuu uu--

Note : " x "＝unknown; " u "＝unchanged; " – "＝unimplemented, read as "0"; "# "＝value depends on condition

10. Instruction Set

Mnemonic Operands	Function	Operation	Status
NOP	No operation	None	
SELT	Load W to OPTR register	W→OPTR	None
SLEEP	Sleep mode	0→WDT, stop OSC	/TO, /PL
WDTCLR	Clear Watchdog timer	0→WDT	/TO, /PF
PTIO M	Control I/O port register	W→PTIO M	None
RET	Return from subroutine	Stack→PC	None
RETI	Return from interrupt	Stack→PC,1→GIE	None
MOVWM M	Store W to Memory	W→M	None
CLRW	Clear working register	0→W	Z
CLRM M	Clear Memory	0→M	Z
SUBWM M,t	Subtract W from Memory	M - W→t (M+/W+1→t)	C, HC, Z
DECM M,t	Decrement Memory	M -1→t	Z
ORWM M,t	Inclu. OR W and Memory	M ∪ W→t	Z
ADDWM M,t	Add W and Memory	W + M→t	C, HC, Z
XORWM M,t	Exclu. OR W and Memory	M ⊕ W→t	Z
ANDWM M,t	AND W and Memory	M ∩ W→t	Z
MOVM M,t	Load Memory	M→t	Z
COMM M,t	Complement Memory	/M→t	Z
INCM M,t	Increment Memory	M + 1→t	Z
DECMZS M,t	Decrement Memory, if zero skip next Memory	M -1→t	None
RRCM M,t	Rotate right Carry bit and Memory	M(n) →M(n-1), C→M(7),M(0)→C	C
RLCM M,t	Rotate left Carry bit and Memory	M(n)→M(n+1), C→M(0),M(7)→C	C
SWAPM M,t	Swap halves Memory	[M(0~3) □M(4~7)]→t	None
INCMZS M,t	Increment Memory, if zero skip next Memory	M + 1→t	None
BCM M,b	Bit clear	0→M(b)	None
BSM M,b	Bit set	1→M(b)	None
BTZS M,b	Bit Test, if zero,skip next Memory	Skip if M(b)=0	None

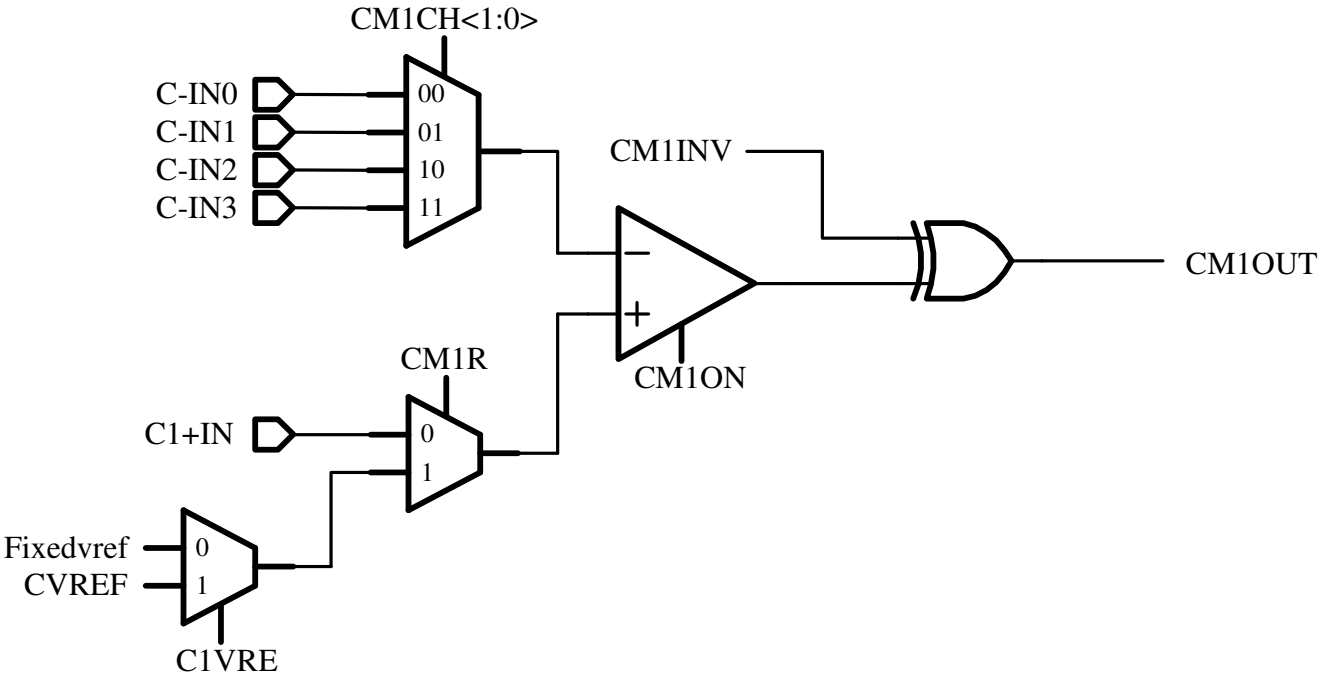
Mnemonic Operands	Function	Operation	Status
BTSS M,b	Bit Test, if set,skip next Memory	Skip if M(b)=1	None
MOVKW I	Load immediate to W	I→W	None
RETKW I	Return, place immediate to W	Stack→PC, I→W	None
ORKW I	Inclu. OR immediate and W	I ∪ W→W	Z
ANDKW I	AND immediate and W	I ∩ W→W	Z
XORKW I	Exclu. OR immediate and W	I ⊕ W→W	Z
SUBKW I	Subtract W from immediate	I - W→W	C,HC,Z
ADDKW I	ADD immediate and W	I + W→W	C,HC,Z
CALL N	CALL subroutine	N→PC, PC+1→Stack	None
GOTO N	JUMP to address	N→PC	None

Note :

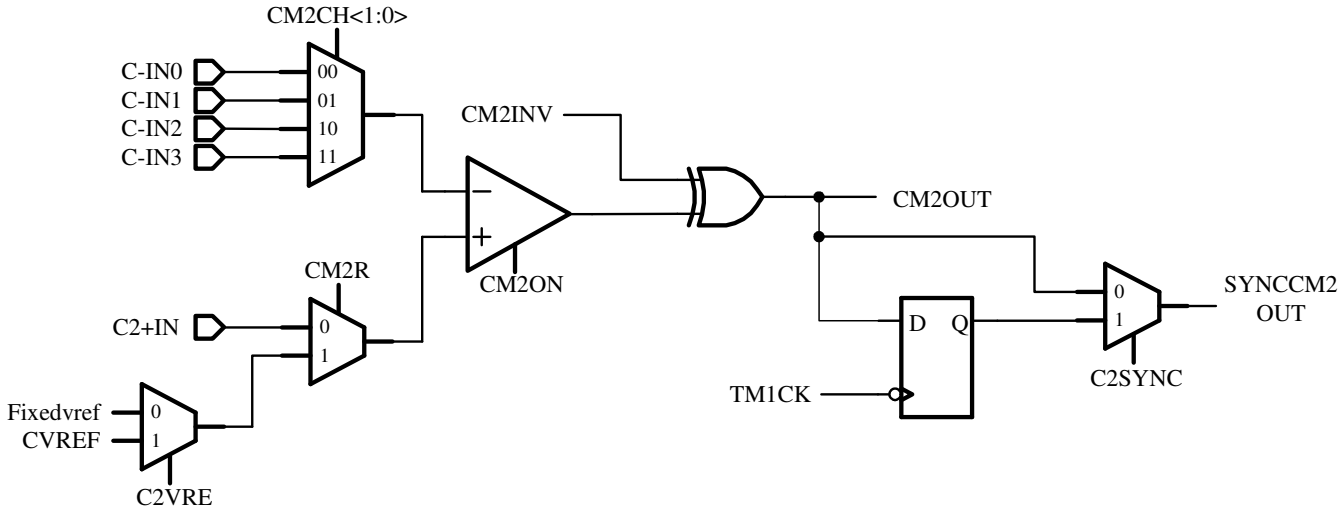
W	:	Working register	b	:	Bit position
WDT	:	Watchdog timer	t	:	Target. 0 : W 1 : M
OPTR	:	OPTR register	M(m)	:	General Memory address
PTIO	:	Control I/O port register	C	:	Carry flag
/TO	:	Timer overflow flag	HC	:	Half carry
/PL	:	Power loss flag	Z	:	Zero flag
PC	:	Program Counter	/	:	Complement
OSC	:	Oscillator	x	:	Don't care
Inclu.	:	Inclusive '∪'	I(i)	:	Immediate data
Exclu.	:	Exclusive '⊕'	N(n)	:	Immediate address
AND	:	Logic AND '∩'			

11. Function Diagram

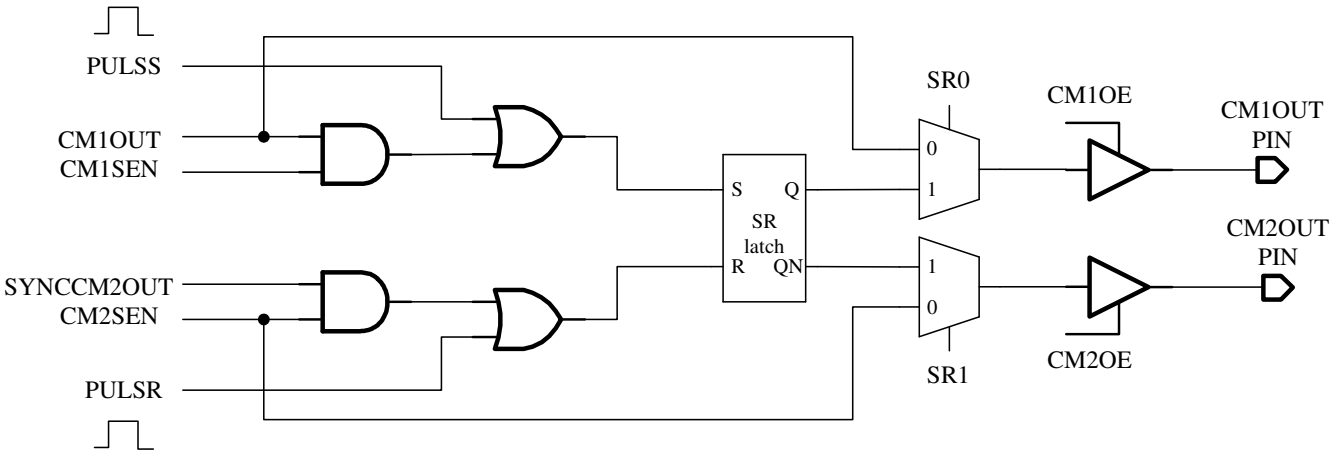
(1) Comparator 1 function diagram



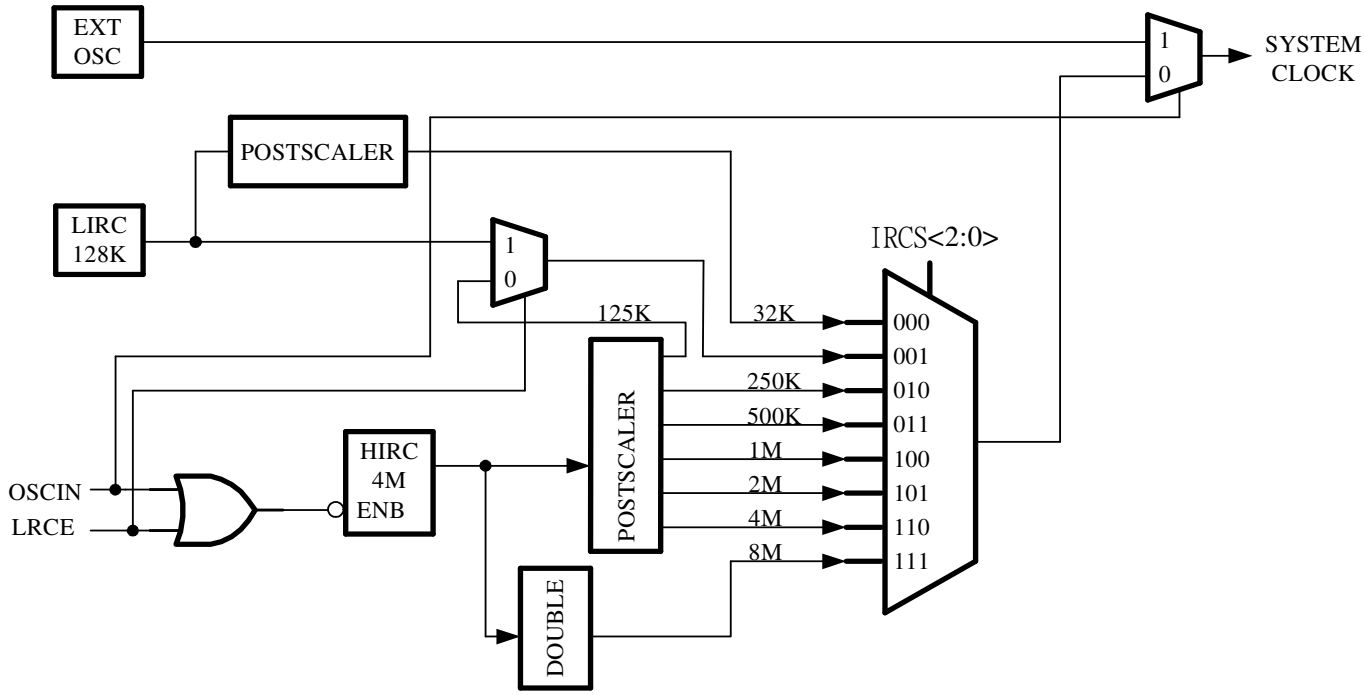
(2) Comparator 2 function diagram



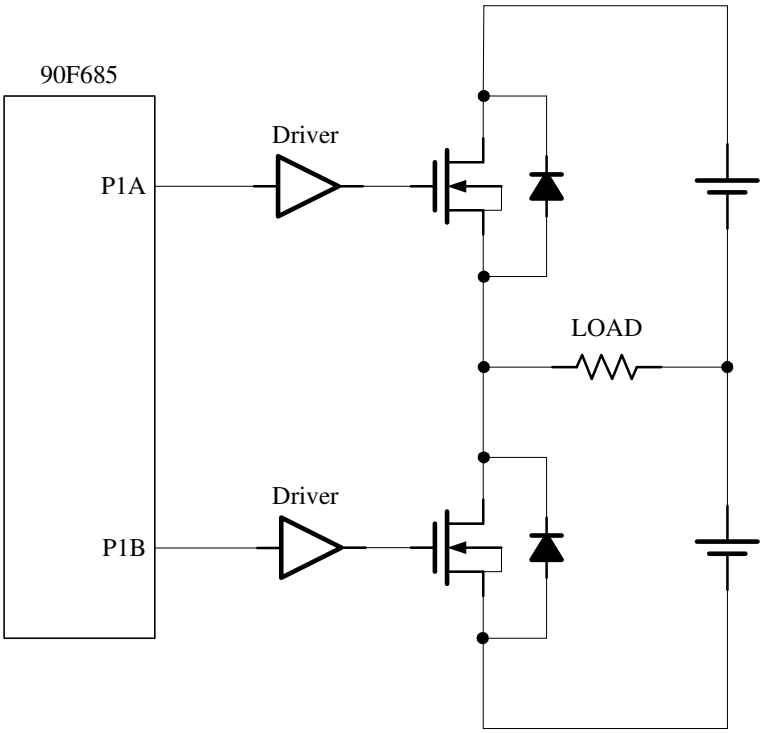
(3) SR latch function diagram

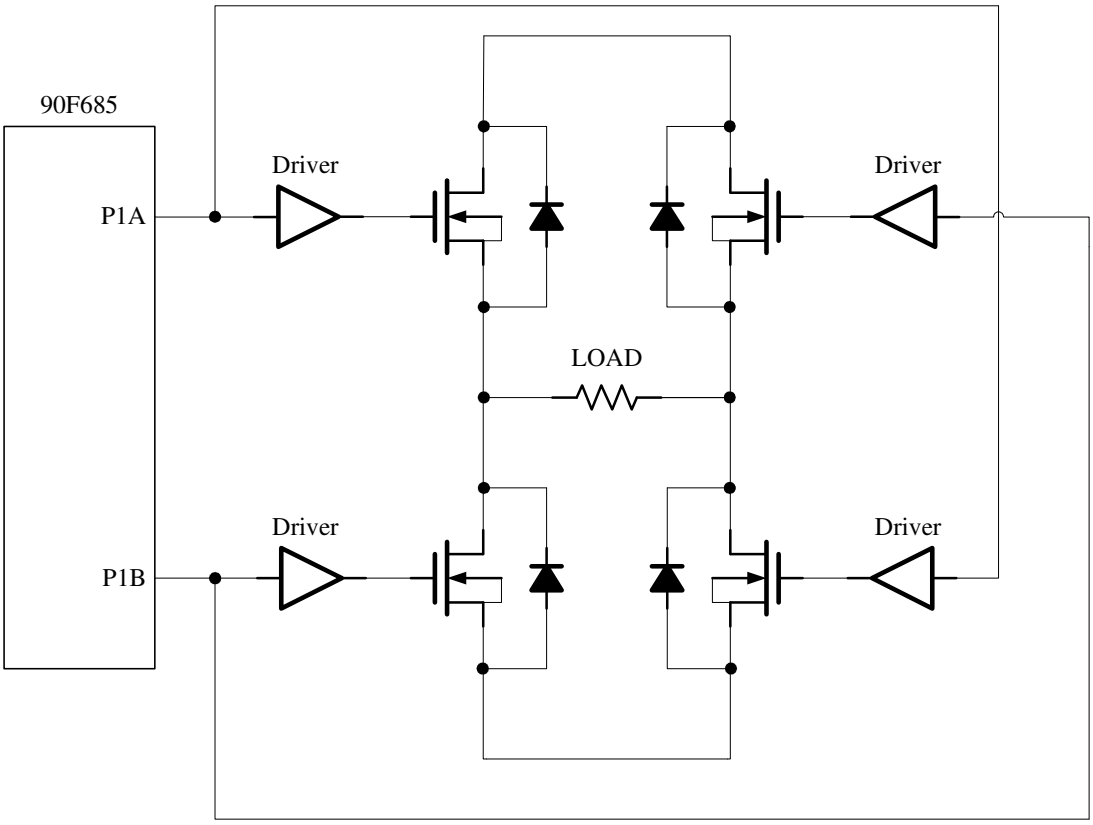


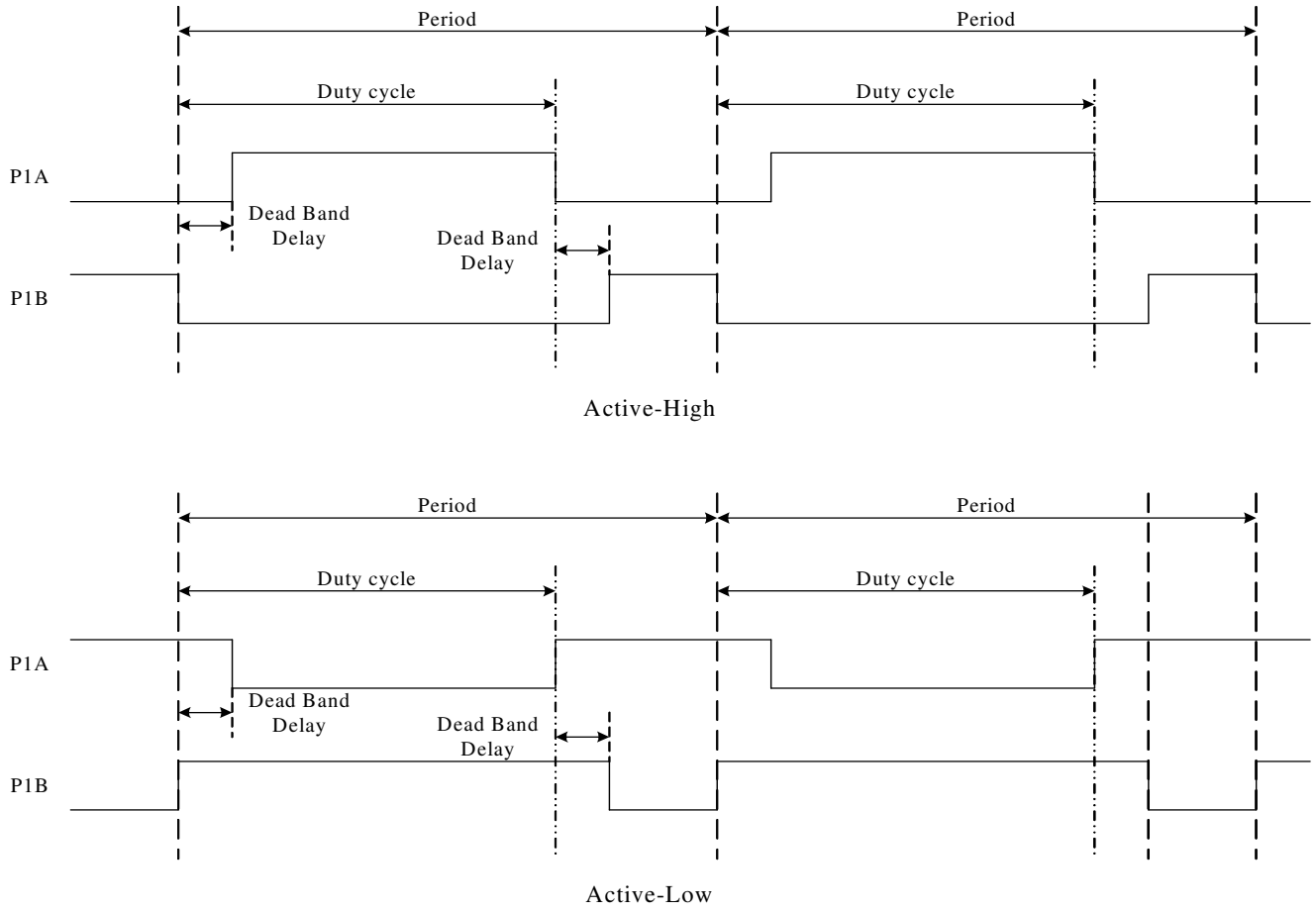
(4)Oscillator control function diagram



(4) PWM Half-Bridge applications diagram



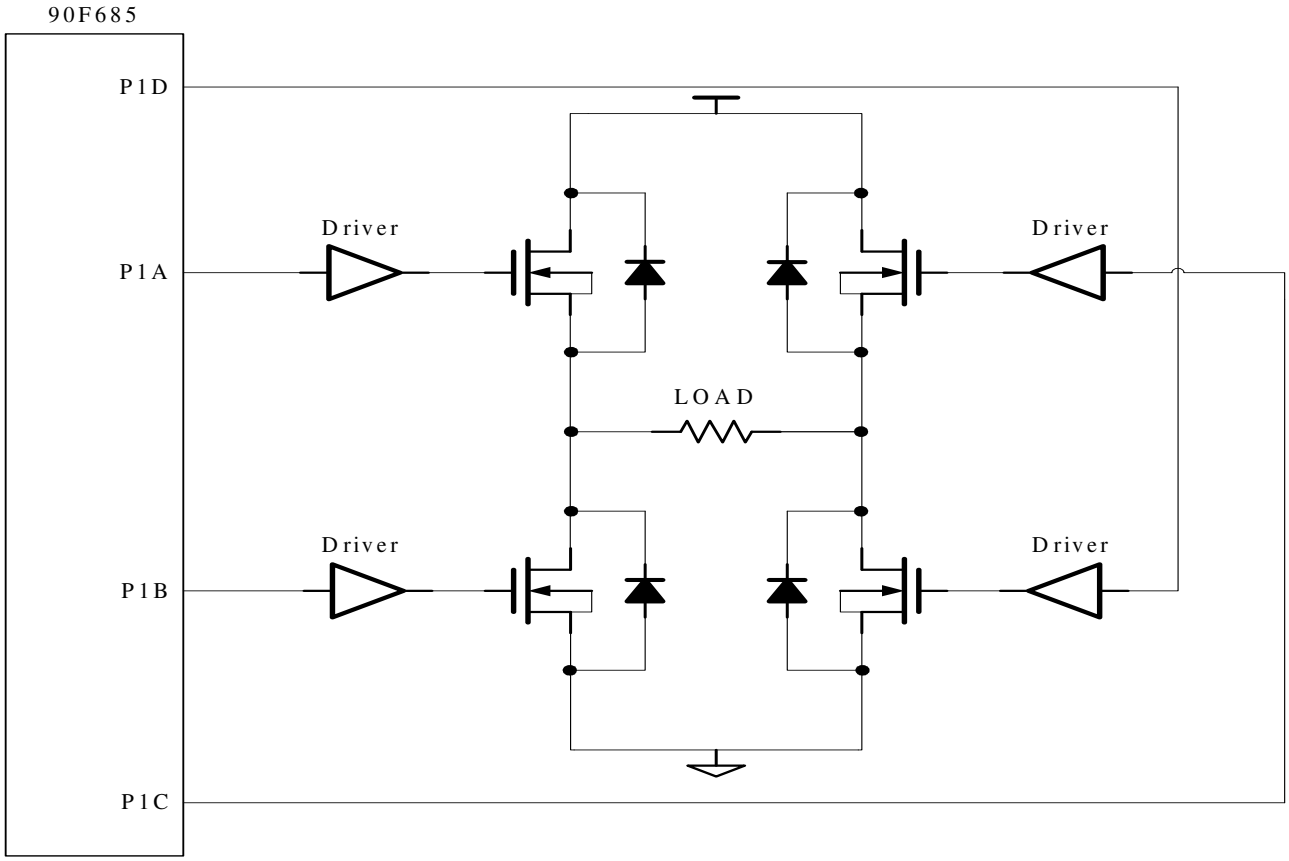


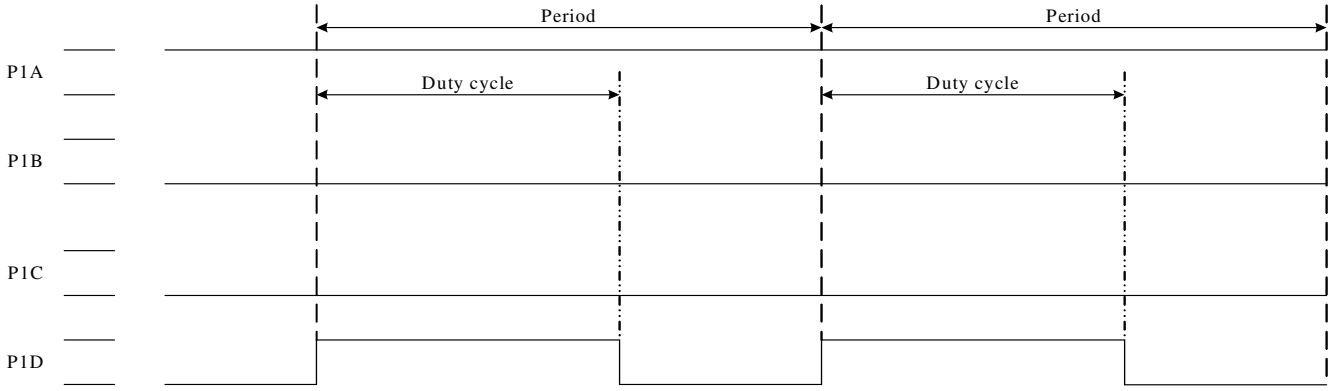


Half-Bridge PWM output

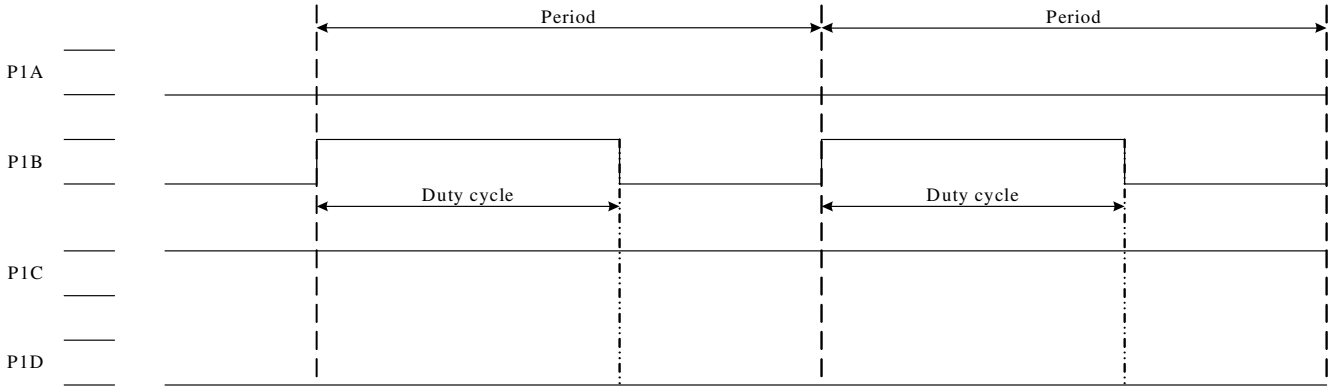
Dead Band Delay = (Fosc/4) x PWMD<6:0>

(5) PWM Full-Bridge applications diagram



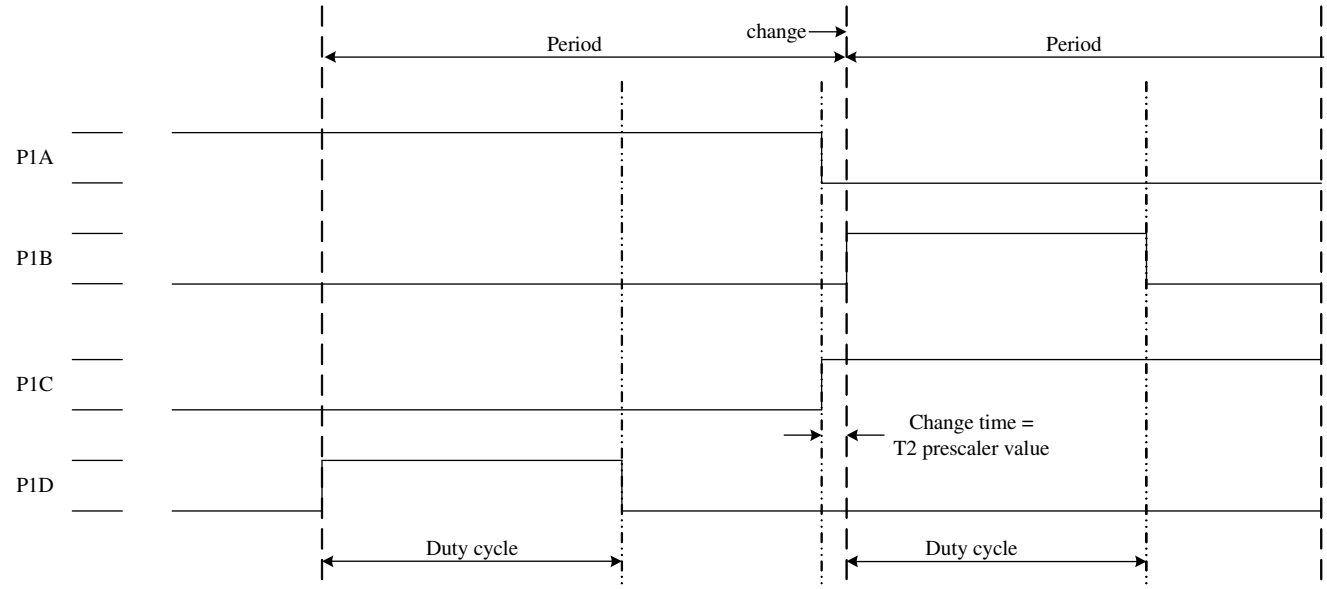


Forward Mode(Active-High-State)



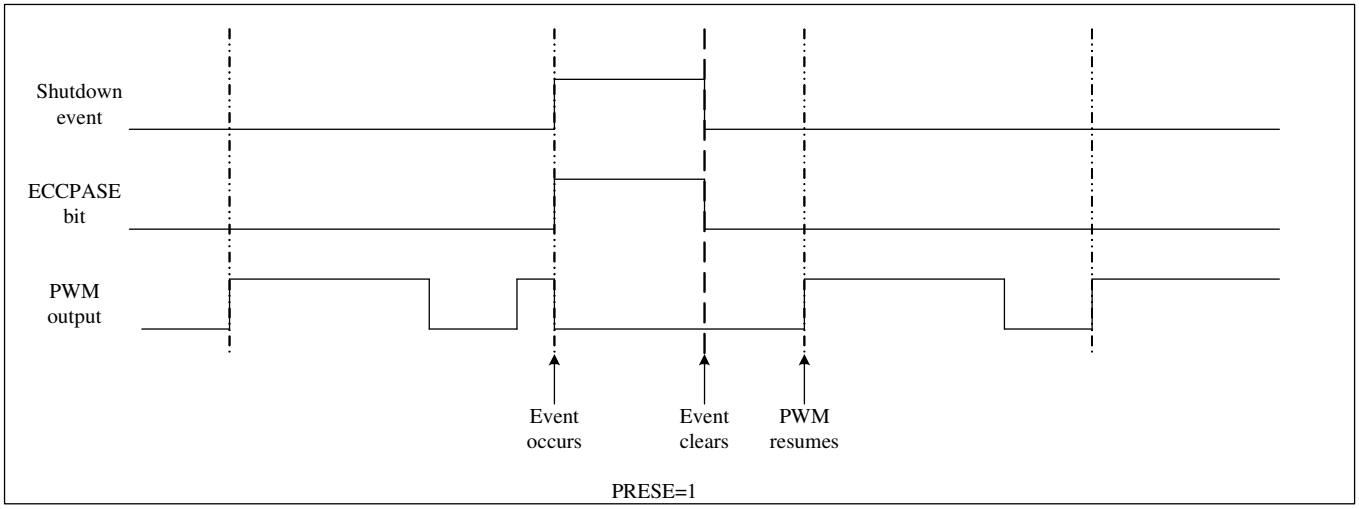
Reverse Mode(Active-High-State)

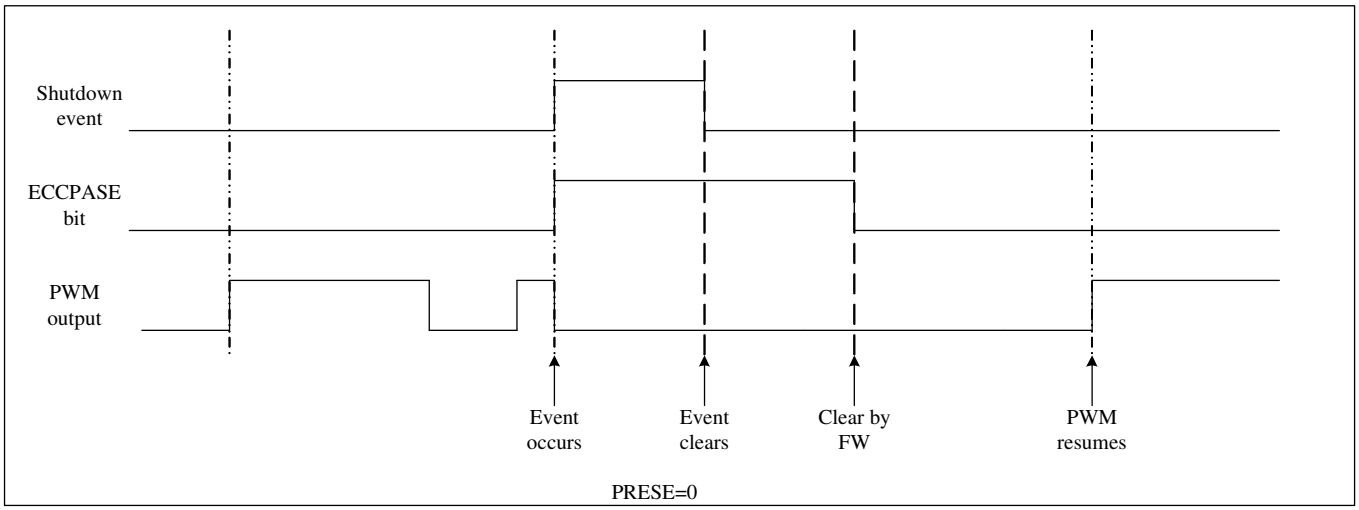
Full-Bridge PWM output



Forward Mode change to Reverse mode (Active-High-State)

(4)PWM auto-shutdown diagram





12. Electrical Characteristics

*Note: Temperature=25℃

Sym	Description	Condition		Min	Typ	Max	Unit
Vdd	Operating voltage			2.3		5.5	V
V_{IL}	Input Low Voltage	Vdd=5V		-0.6		1.0	V
V_{IH}	Input high Voltage PA, PB,PC	Vdd=5V Vdd=3V		2.0 1.5		Vdd Vdd	V
I_{IL}	Input leakage current	Vdd=5V				+/-1	μA
V_{OL}	Output Low Voltage PA(ext PA3), PB, PC	Vdd=5V, I_{OL}=20mA Vdd=5V, I_{OL}=5mA			0.6 0.2		V V
V_{OH}	Output High Voltage PA(ext PA3), PB, PC	Vdd=5V, I_{OH}= -20mA Vdd=5V, I_{OH}= -5mA			3.3 4.5		V V
Rph	PA(ext PA3),PB pullhigh resister	Vdd=5V Vdd=3V			20k 55k		Ω
I_{slp}	**Sleep current** OSC TYPE:IRC PUT:75ms WDT:Enable PED:Disable	V_{dd}＝2.5 V V_{dd}＝3.0 V V_{dd}＝4.0 V V_{dd}＝5.0 V V_{dd}＝6.0 V			1 1.5 3.6 6.4 10.2		μA μA μA μA μA
Imax	**Max output driver** PA(ext PA3), PB, PC	Vdd=5V	Sourse current Sink current		30 50		mA
		Vdd=3V	Sourse current Sink current		10 20		mA
Idd 1	**Operation Current 1** OSC TYPE:HF PUT:75ms WDT:Enable PED:Disable No load	4MHz	Vdd=5V Vdd=3V		1.5 400		mA uA
		10MHz	Vdd=5V Vdd=3V		2.0 750		mA uA
		20MHz	Vdd=5V Vdd=3V		3 1.5		mA mA
Idd 2	**Operation Current 2** OSC TYPE:LF with 50p PUT:75ms WDT,PED:Disable No load	32KHz	V_{dd}＝2.5 V V_{dd}＝3.0 V V_{dd}＝5.0 V		15 20 90		uA uA uA

Sym	Description	Condition		Min	Typ	Max	Unit
Idd 3	**Operation Current 3** OSC TYPE:RC PUT:0ms WDT,PED:Disable No load	4MHz	Vdd=5.0v V_{dd}=3.0		1.5 700		mA uA
		500kHz	Vdd=5.0v V_{dd}=3.0		300 100		uA uA
Idd 4	**Operation Current 4** OSC TYPE:IRC PUT:0ms WDT,PED:Disable No load	4MHz	V_{dd}=2.5 V V_{dd}=3.0 V V_{dd}=5.0 V		300 400 1000		uA
Idd 5	**Operation Current 5** OSC TYPE:IRC PUT:0ms WDT,PED:Disable No load	1MHz	V_{dd}=2.5 V V_{dd}=3.0 V V_{dd}=5.0 V		190 220 410		uA
Idd 6	**Operation Current 6** OSC TYPE:LIRC PUT:0ms WDT,PED:Disable No load	32kHz	V_{dd}=2.5 V V_{dd}=3.0 V V_{dd}=5.0 V		11 18 65		uA
Twdt	The basic WDT time-out cycle time	V_{dd}=2.5 V V_{dd}=3.0 V V_{dd}=4.0 V V_{dd}=5.0 V V_{dd}=5.5 V			24.3 22.3 19.6 17.9 17.4		mS mS mS mS mS

12. External Capacitor Selection For Crystal Oscillator

Osc. Type	Resonator Freq.	C1	C2
HF	20 MHz	5 pF ~10 pF	10 pF ~30 pF
	10 MHz	10 pF ~50 pF	20 pF ~100 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
XT	10 MHz	10 pF ~30 pF	10 pF ~50 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
	1 MHz	10 pF ~30 pF	20 pF ~50 pF
LF	1 MHz	3 pF ~5 pF	3 pF ~5 pF
	455 K	10 pF ~30 pF	20 pF ~50 pF
	32 K	10 pF ~20 pF	15 pF ~30 pF